CLAIMS

1. A semiconductor testing apparatus which tests the gradation output voltage characteristics of a semiconductor integrated circuit for outputting a gradation output voltage through each of a plurality of output terminals and which comprises plural pieces of output voltage testing means each corresponding to each of said output terminals, wherein said output voltage testing means comprises:

test voltage inputting means for inputting a voltage to be tested which is obtained from a gradation output voltage;

comparison voltage generating means for generating a comparison voltage to be compared with the voltage to be tested, on the basis of comparison voltage generation data provided from comparison voltage generation data inputting means; and

comparing means for comparing the voltage to be tested with the comparison voltage; and wherein

said comparison voltage generation data is generated by adding common comparison voltage generation data shared with the other pieces of output voltage testing means to individual comparison voltage generation data provided for each piece of output voltage testing means in order to correct an intrinsic error in each piece of comparing means.

2. A semiconductor testing apparatus according to Claim 1,

wherein said comparison voltage generation data inputting means comprises:

common comparison voltage generation data inputting means for inputting the common comparison voltage generation data;

individual comparison voltage generation data inputting means for inputting the individual comparison voltage generation data; and

an adder for adding the common comparison voltage generation data to the individual comparison voltage generation data; and wherein

the result of the addition in said adder is provided as said comparison voltage generation data to the comparison voltage generating means.

3. A semiconductor testing apparatus according to Claim 1, wherein:

the output voltage testing means is composed of an electronic circuit for testing the voltage to be tested;

the test voltage inputting means is composed of an electronic circuit for inputting the voltage to be tested; and

the comparison voltage generation data inputting means is composed of an electronic circuit for inputting the comparison voltage generation data.

4. A semiconductor testing apparatus according to Claim 2, wherein:

the common comparison voltage generation data inputting means is composed of an electronic circuit for inputting the common comparison voltage generation data; and

the individual comparison voltage generation data inputting means is composed of an electronic circuit for inputting the individual comparison voltage generation data.

5. A semiconductor testing apparatus according to Claim 2, wherein said comparing means comprises:

a high level comparator for comparing and detecting whether the voltage to be tested is at or below an upper allowable limit relative to the comparison voltage or not; and

a low level comparator for comparing and detecting whether the voltage to be tested is at or above a lower allowable limit relative to the comparison voltage or not; and wherein:

a high level comparison voltage generated by comparison voltage generation data inputting means and comparison voltage generating means corresponding to the high level comparator is provided to the high level comparator; and

a low level comparison voltage generated by comparison voltage generation data inputting means and comparison voltage generating means corresponding to the low level comparator is provided to the low level comparator.

6. A semiconductor testing apparatus according to Claim 5, further comprising an integrated circuit driving section for driving said semiconductor integrated circuit.

7. A semiconductor testing apparatus according to Claim 6, wherein said semiconductor integrated circuit is composed of a semiconductor integrated circuit for liquid crystal driving.

8. A semiconductor testing apparatus according to Claim 1, wherein said comparing means comprises:

a high level comparator for comparing and detecting whether the voltage to be tested is at or below an upper allowable limit relative to the comparison voltage or not; and

a low level comparator for comparing and detecting whether the voltage to be tested is at or above a lower allowable limit relative to the comparison voltage or not; and wherein:

a high level comparison voltage generated by comparison voltage generation data inputting means and comparison voltage generating means corresponding to the high level comparator is provided to the high level comparator; and

a low level comparison voltage generated by comparison voltage generation data inputting means and comparison voltage generating means corresponding to the low level comparator is provided to the low level comparator.

9. A semiconductor testing apparatus according to Claim 8, further comprising correction data generating means for setting and storing said individual comparison voltage generation data and for outputting the individual comparison voltage generation data to the comparison voltage generation data inputting means.

10. A semiconductor testing apparatus according to Claim 9, wherein the correction data generating means is composed of an electronic circuit for generating the individual comparison voltage generation data.

11. A semiconductor testing apparatus according to Claim 1, further comprising correction data generating means for setting and storing said individual comparison voltage generation data and for outputting the individual comparison voltage generation data to the comparison voltage generation data inputting means.

12. A semiconductor testing apparatus according to Claim 11, wherein said correction data generating means is provided for each piece of output voltage testing means.

13. A semiconductor testing apparatus according to Claim 12, further comprising an integrated circuit driving section for driving said semiconductor integrated circuit.

14. A semiconductor testing apparatus according to Claim 13, wherein said semiconductor integrated circuit is composed of a semiconductor integrated circuit for liquid crystal driving.

15. A semiconductor testing apparatus according to Claim 1, further comprising:

expected voltage generating means for outputting an expected gradation voltage corresponding to said gradation output voltage; and

voltage difference detecting means for acquiring the difference between the gradation output voltage and the expected gradation voltage and then outputting the difference to the test voltage inputting means.

16. A semiconductor testing apparatus according to Claim 15, wherein said expected voltage generating means comprises:

ideal value input data storing means for storing ideal value input data for the expected gradation voltage;

correction value input data storing means for storing correction value input data for correcting the expected gradation voltage;

an adder for adding the ideal value input data to the correction value input data and then outputting the expected voltage data; and

expected voltage outputting means for generating an expected gradation voltage based on the expected voltage data and then providing the expected gradation voltage to the voltage difference detecting means.

17. A semiconductor testing apparatus according to Claim 16, wherein said comparison voltage generating means comprises a digital-to-analogue converter, while said expected voltage outputting means comprises a digital-to-analogue converter, and wherein the digital-to-analogue converter provided in the expected voltage outputting means has a higher resolution than the digital-to-analogue converter provided in the comparison voltage generating means.

18. A semiconductor testing apparatus according to Claim 15, wherein said expected voltage generating means is composed of an electronic circuit for generating the expected gradation voltage.

19. A semiconductor testing apparatus according to Claim 16, wherein:

said ideal value input data storing means is composed of an ideal value input data memory device; and

said correction value input data storing means is composed of a correction value input data memory device.

20. A semiconductor testing apparatus according to Claim 17, further comprising an integrated circuit driving section for driving said semiconductor integrated circuit.

21. A semiconductor testing apparatus according to Claim 20, wherein said semiconductor integrated circuit is composed of a semiconductor integrated circuit for liquid crystal driving.

22. A semiconductor testing apparatus according to Claim 15, further comprising amplifying means for amplifying an output of said voltage difference detecting means and for providing the amplified output to the test voltage inputting means.

23. A semiconductor testing apparatus according to Claim 22, wherein said voltage difference detecting means is composed of a subtractor, while said amplifying means is composed of an amplifier.

24. A semiconductor testing apparatus according to Claim 22, further comprising a first correction switch a common terminal of which is connected to the test voltage inputting means, a first independent terminal of which is connected to the output terminal of the amplifying means, and a second independent terminal of which is connected to a fixed potential terminal, wherein

said first correction switch connects the test voltage

inputting means to the amplifying means when said gradation output voltage is to be tested, and connects the test voltage inputting means to the fixed potential terminal when the individual comparison voltage generation data is to be set and corrected in order to correct said comparison voltage.

25. A semiconductor testing apparatus according to Claim 24, wherein said semiconductor testing apparatus is constructed as a module.

26. A semiconductor testing apparatus according to Claim 25, further comprising an integrated circuit driving section for driving said semiconductor integrated circuit.

27. A semiconductor testing apparatus according to Claim 26, wherein said semiconductor integrated circuit is composed of a semiconductor integrated circuit for liquid crystal driving.

28. A semiconductor testing apparatus according to Claim 22, further comprising a second correction switch a common terminal of which is connected to the voltage difference detecting means, a first independent terminal of which is connected to the output terminal of the semiconductor integrated circuit, and a second independent terminal of which is connected to precision voltage generating means, wherein

said second correction switch connects the voltage difference detecting means to the semiconductor integrated circuit when said gradation output voltage is to be tested, and connects the voltage difference detecting means to the precision voltage generating means when said expected voltage generating means is to be corrected.

29. A semiconductor testing apparatus according to Claim 28, wherein said semiconductor testing apparatus is constructed as a module.

30. A semiconductor testing apparatus according to Claim 29, further comprising an integrated circuit driving section for driving said semiconductor integrated circuit.

31. A semiconductor testing apparatus according to Claim 30, wherein said semiconductor integrated circuit is composed of a semiconductor integrated circuit for liquid crystal driving.

32. A semiconductor testing method for testing the gradation output voltage characteristics of a semiconductor integrated circuit for outputting a gradation output voltage through each of a plurality of output terminals, comprising the steps of:

providing a voltage to be tested which is based on the difference between said gradation output voltage and an expected

gradation voltage corresponding to an ideal value for the gradation output voltage, into plural pieces of output voltage testing means each provided corresponding to each of said output terminals; and

comparing a comparison voltage which is to be compared with said voltage to be tested, with said voltage to be tested and thereby testing the gradation output voltage by means of said output voltage testing means; wherein

said comparison voltage is corrected in each piece of output voltage testing means in order to correct the intrinsic error of a digital-to-analogue converter provided in each piece of output voltage testing means.

33. A semiconductor testing method according to Claim 32, wherein said expected gradation voltage is corrected in order to correct the intrinsic error of a digital-to-analogue converter provided in expected voltage generating means for generating an expected gradation voltage.